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U.S. **UTILITY** Patent Application

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 APPLICATION NO.
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 ART UNIT
 EXAMINER

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 25-7-436
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Angel Pepe James Yamaguchi

Stackable layers containing encapsulated integrated circuit chips with one or more overlying interconnect layers and a method of making the same

PTO-204 12/99

ISSUING CLASSIFICATION						
ORIGINA	L	CROSS REFERENCE(S)				
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INTERNATIONAL	CLASSIFICATION					
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TERMINAL	DRAWINGS			CLAIMS ALLOWED	
└── DISCLAIMER	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
The term of this patent subsequent to (date)				NOTICE OF ALLOWANCE MAILED	
has been disclaimed.	(Assistant Examiner)		(Date)		
The term of this patent shall not extend beyond the expiration date					
of U.S Patent. No.				ISSUE FEE	
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WARNING:				· · · · · · · · · · · · · · · · · · ·	
The information disclosed herein may be rest Possession outside the U.S. Patent & Tradem					15, Sections 122, 181 and 366
orm PTO-436A Rev. 6/99)			FILED WITH:	DISK (CRF)	FICHE CD-RO

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